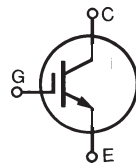
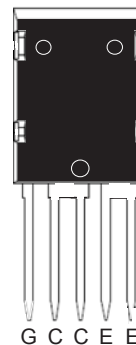


Medium speed low V_{sat} PT
IGBTs 5-40 kHz switching



V_{CES} = 600V
I_{C110} = 90A
V_{CE(sat)} ≤ 1.50V
t_{fi(typ)} = 183ns



G = Gate C = Collector
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
V _{CES}	T _J = 25°C to 150°C	600	V
V _{CGR}	T _J = 25°C to 150°C, R _{GE} = 1MΩ	600	V
V _{GES}	Continuous	±20	V
V _{GEM}	Transient	±30	V
I _{C25}	T _C = 25°C (limited by leads)	150	A
I _{C110}	T _C = 110°C (chip capability)	90	A
I _{CM}	T _C = 25°C, 1ms	600	A
SSOA (RBSOA)	V _{GE} = 15V, T _{vj} = 125°C, R _G = 1Ω Clamped inductive load @ V _{CE} ≤ 600V	I _{CM} = 300	A
P _C	T _C = 25°C	400	W
T _J		-55 ... +150	°C
T _{JM}		150	°C
T _{stg}		-55 ... +150	°C
T _L	Maximum lead temperature for soldering	300	°C
T _{SOLD}	Plastic body for 10s	260	°C
V _{ISOL}	50/60Hz, RMS, 1 minute	2500	V~
	I _{ISOL} ≤ 1mA t = 1s	3000	V~
F _C	Mounting force	20..120/4.5..27	N/lb.
Weight		8	g

Symbol	Test Conditions (T _J = 25°C, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	I _C = 250μA, V _{GE} = 0V	600		V
V_{GE(th)}	I _C = 250μA, V _{CE} = V _{GE}	3.0		V
I_{CES}	V _{CE} = V _{CES} V _{GE} = 0V T _J = 125°C			200 μA 2 mA
I_{GES}	V _{CE} = 0V, V _{GE} = ±20V			±100 nA
V_{CE(sat)}	I _C = 100A, V _{GE} = 15V, Note 1 I _C = 200A T _J = 125°C		1.35 1.65 1.75	V V V

Features

- Silocon chip on Direct-Copper Bond (DCB) substrate
- Isolated mounting surface
- Square RBSOA
- High current handling capability
- 2500V electrical isolation

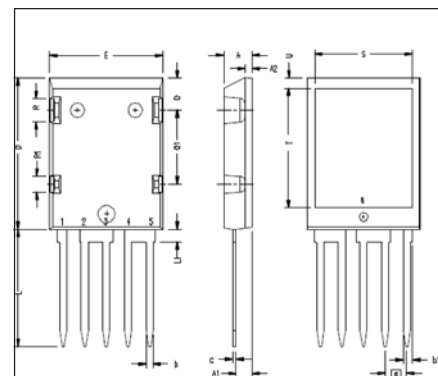
Advantages

- High power density
- Low gate drive requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 60\text{A}, V_{CE} = 10\text{V}$, Note 1	95	160	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		26	nF
C_{oes}			1260	pF
C_{res}			97	pF
Q_g	$I_C = 100\text{A}, V_{GE} = 15\text{V}, V_{CE} = 0.5 \cdot V_{CES}$		750	nC
Q_{ge}			115	nC
Q_{gc}			245	nC
$t_{d(on)}$	Inductive load, $T_J = 25^\circ\text{C}$ $I_C = 100\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 300\text{V}, R_G = 1\Omega$		44	ns
t_{ri}			83	ns
E_{on}			1.6	mJ
$t_{d(off)}$			310	450 ns
t_{fi}			183	300 ns
E_{off}			2.9	4.5 mJ
$t_{d(on)}$	Inductive load, $T_J = 125^\circ\text{C}$ $I_C = 100\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 300\text{V}, R_G = 1\Omega$		42	ns
t_{ri}			80	ns
E_{on}			2.4	mJ
$t_{d(off)}$			430	ns
t_{fi}			300	ns
E_{off}			4.2	mJ
R_{thJC}			0.31	$^\circ\text{C/W}$
R_{thCS}		0.11		$^\circ\text{C/W}$



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.055	1.17	1.40
b	.045	.055	1.14	1.40
b1	.063	.072	1.60	1.83
c	.020	.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
L	.780	.820	19.81	20.83
L1	.050	.102	2.03	2.59
Q	.210	.235	5.33	5.97
Q1	.490	.513	12.45	13.03
R	.150	.180	3.81	4.57
R1	.100	.130	2.54	3.30
S	.608	.690	15.47	17.53
T	.801	.821	20.34	20.85
U	.085	.060	1.65	2.03

NOTE: BOTTOM HEATSINK MEETS 2,500Vrms ISOLATION TO THE OTHER PINS.

Note 1: Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

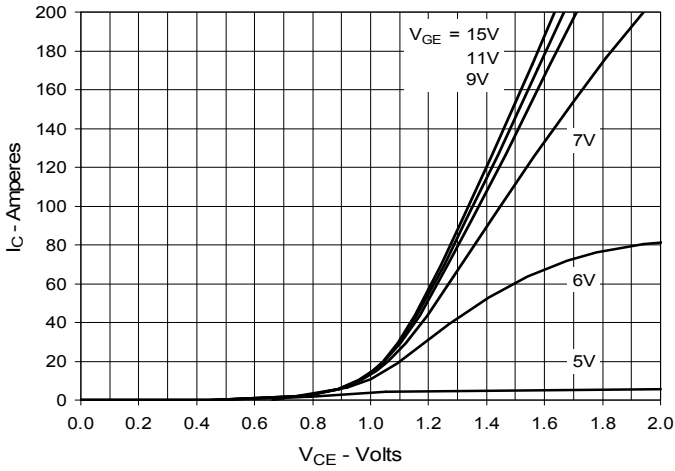
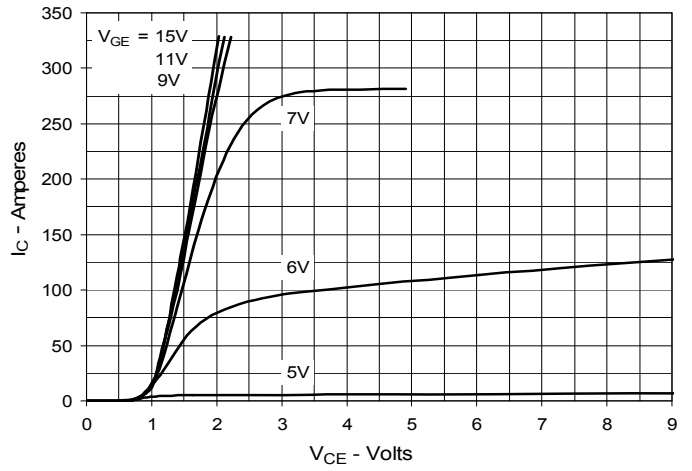
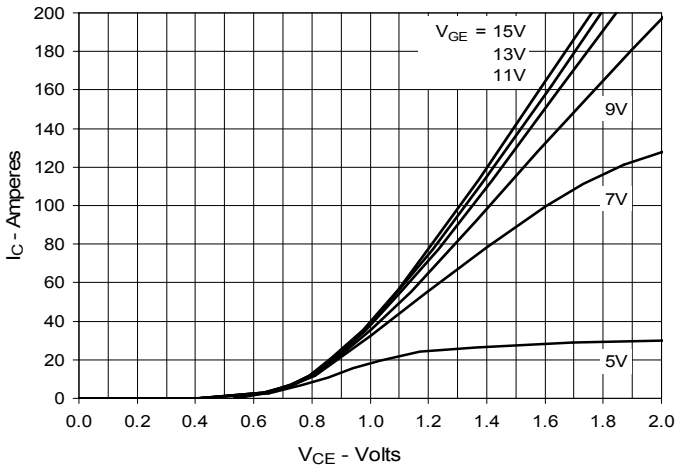
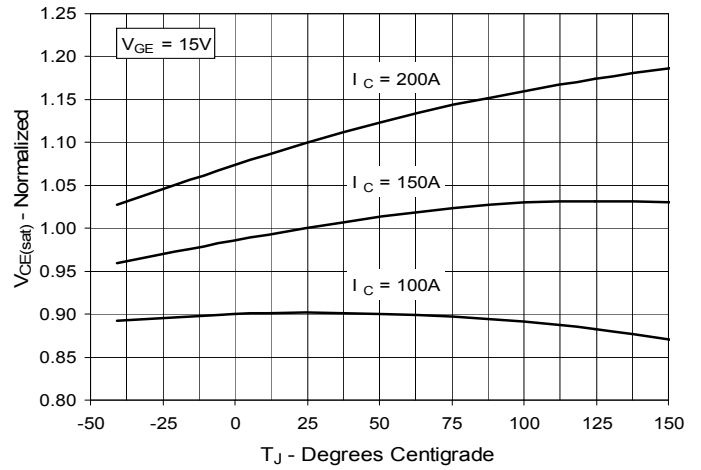
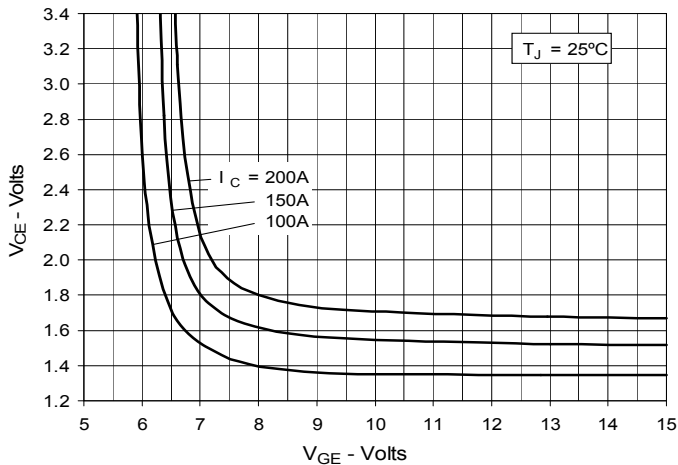
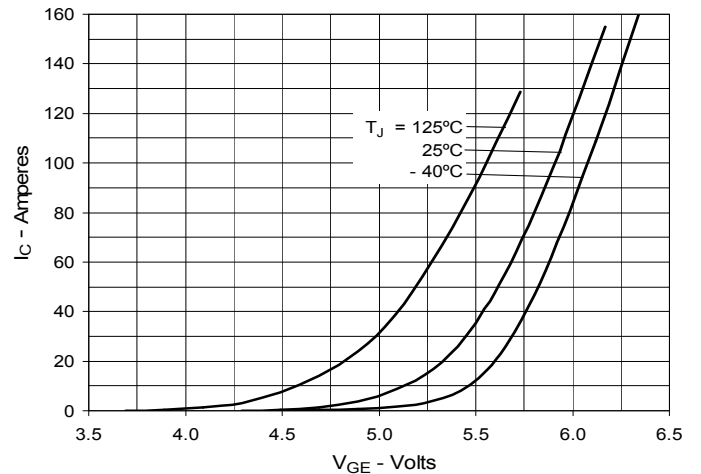
Fig. 1. Output Characteristics @ 25°C

Fig. 2. Extended Output Characteristics @ 25°C

Fig. 3. Output Characteristics @ 125°C

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

Fig. 6. Input Admittance


Fig. 7. Transconductance

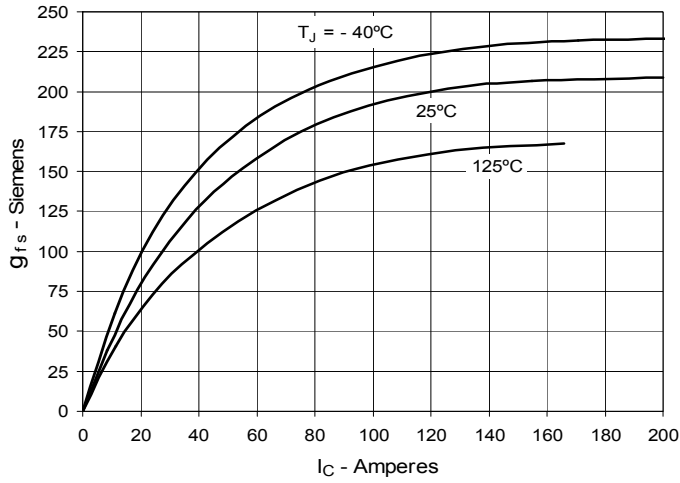


Fig. 8. Gate Charge

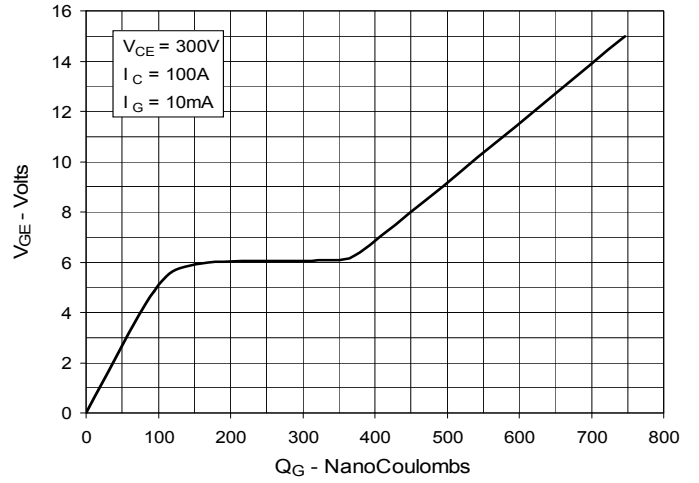


Fig. 9. Capacitance

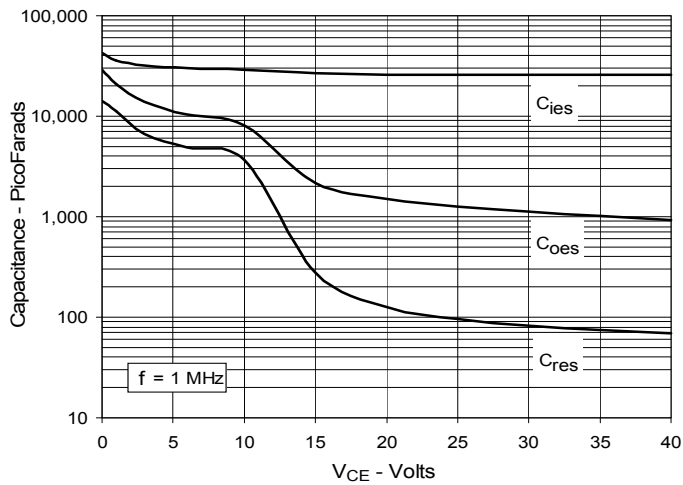


Fig. 10. Reverse-Bias Safe Operating Area

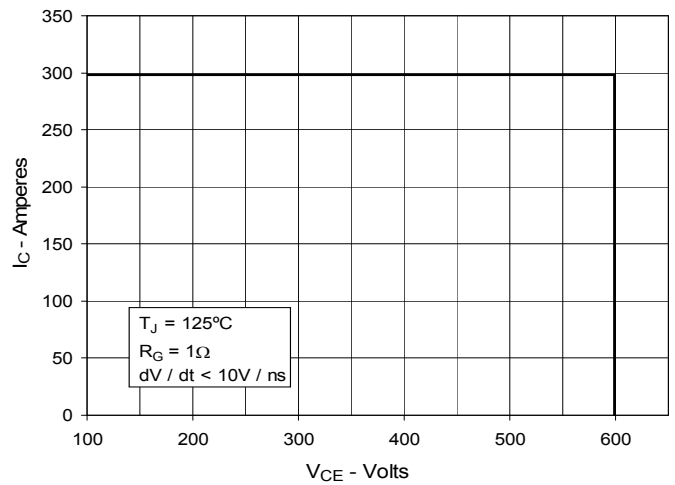
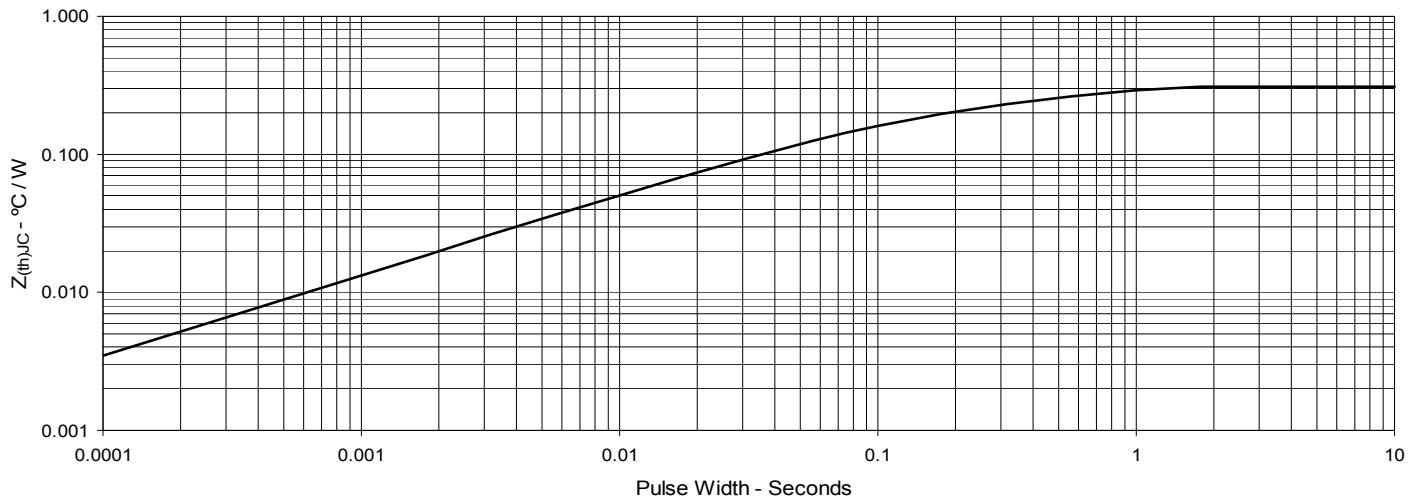
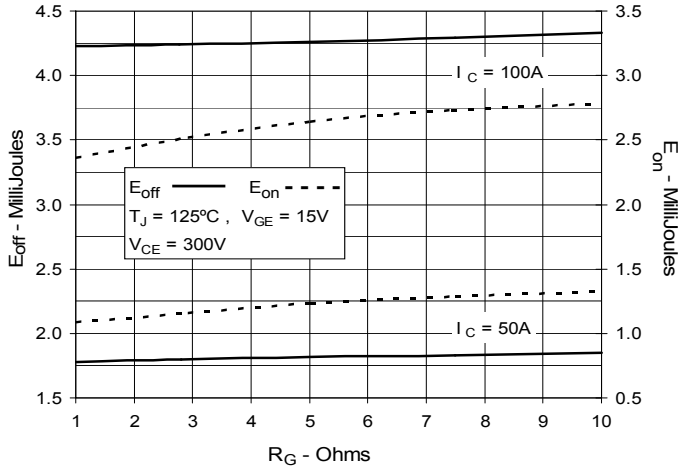
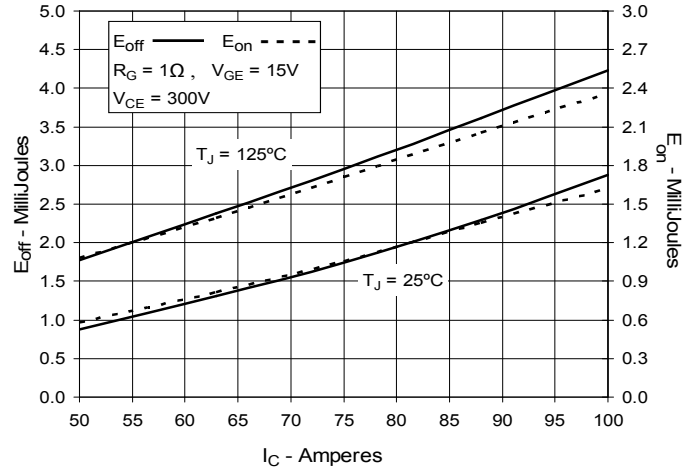
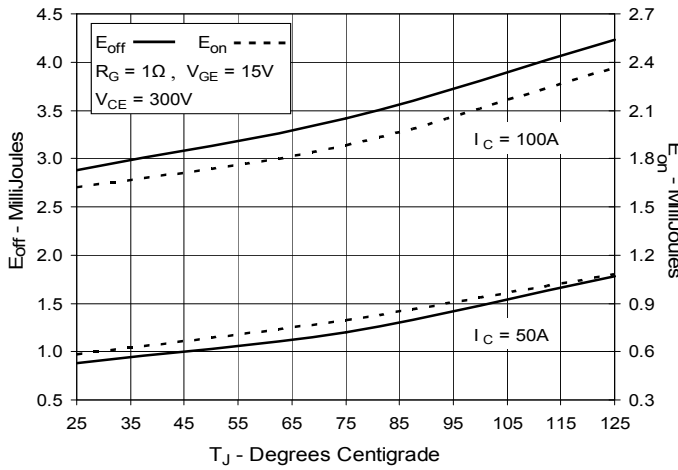
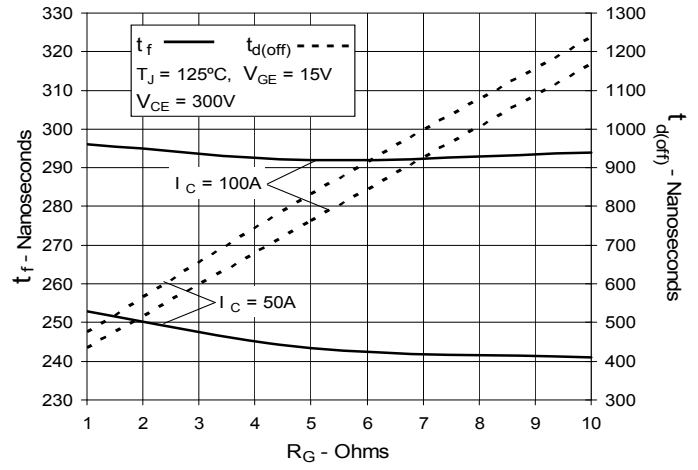
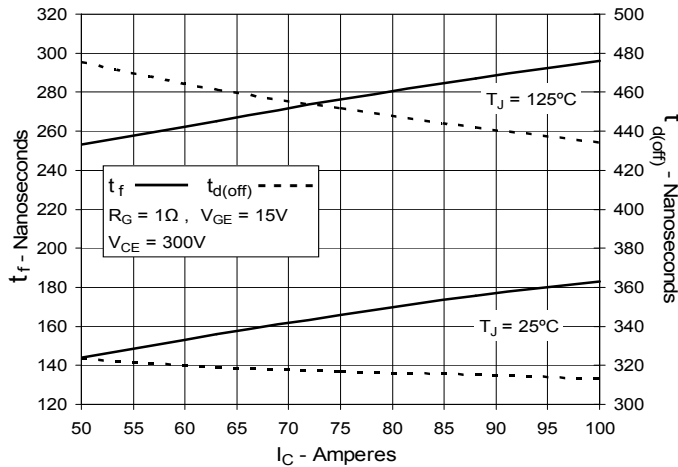
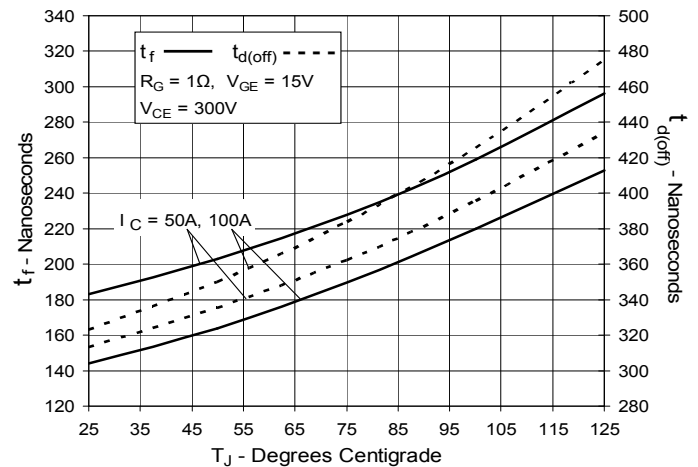


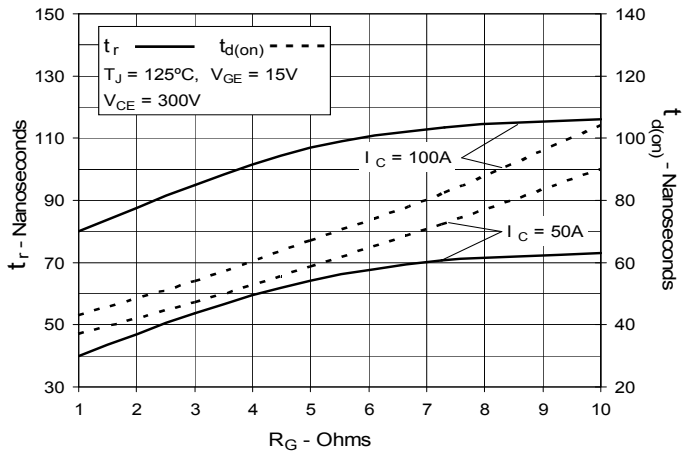
Fig. 11. Maximum Transient Thermal Impedance



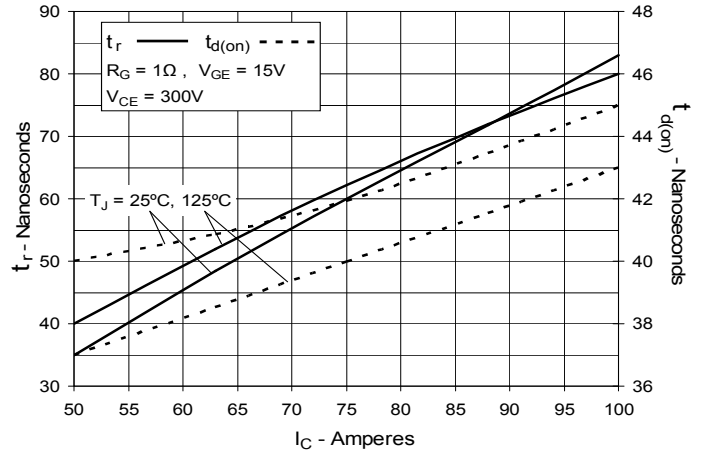
IXYS reserves the right to change limits, test conditions, and dimensions.

**Fig. 12. Inductive Switching
Energy Loss vs. Gate Resistance**

**Fig. 13. Inductive Switching
Energy Loss vs. Collector Current**

**Fig. 14. Inductive Switching
Energy Loss vs. Junction Temperature**

**Fig. 15. Inductive Turn-off
Switching Times vs. Gate Resistance**

**Fig. 16. Inductive Turn-off
Switching Times vs. Collector Current**

**Fig. 17. Inductive Turn-off
Switching Times vs. Junction Temperature**


**Fig. 18. Inductive Turn-on
Switching Times vs. Gate Resistance**



**Fig. 19. Inductive Turn-on
Switching Times vs. Collector Current**



**Fig. 20. Inductive Turn-on
Switching Times vs. Junction Temperature**

