MAX14934–MAX14936

Four-Channel, 5kV$_{RMS}$ Digital Isolators

General Description

The MAX14934–MAX14936 are a family of four-channel, 5kV$_{RMS}$ digital isolators utilizing Maxim's proprietary process technology. For applications requiring 2.75kV$_{RMS}$ of isolation, see the MAX14930–MAX14932. The MAX14934–MAX14936 family transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C.

The MAX14934–MAX14936 family offers all three possible unidirectional channel configurations to accommodate any four-channel design, including SPI, RS-232, RS-485, and large digital IO modules. For applications requiring bidirectional channels, such as I^{2}C, refer to the MAX14937.

Devices are available with data rates from DC up to 1Mbps, 25Mbps, or 150Mbps. Each device is also available in either a default high or default low configuration. The default is the state an output goes to when its input is unpowered. See the *Ordering Information/Selector Guide* for the suffixes associated with each option.

Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators.

The MAX14934–MAX14936 are available in a 16-pin wide body (10.3mm x 7.5mm) SOIC package. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

***Ordering Information/Selector Guide* appears at end of data sheet.**

Benefits and Features

- Robust Galvanic Isolation of Digital Signals
  - Withstands 5kV$_{RMS}$ for 60s (V$_{ISO}$)
  - Continuously Withstands 848V$_{RMS}$ (V$_{IOWM}$)
  - 1200V$_P$ Repetitive Peak Voltage (V$_{IORM}$)
  - Withstands ±10kV Surge per IEC 61000-4-5
- Interfaces Directly with Most Micros and FPGAs
  - Accepts 1.71V to 5.5V Supplies
- Many Options Support Broad Applications
  - 3 Data Rates (1Mbps, 25Mbps, 150Mbps)
  - 3 Channel Direction Configuration
  - 2 Output Default States (High or Low)
- Low Power Consumption at High Data Rates
  At 1.8V:
  - 2.5mA per Channel Typical at 1Mbps
  - 5.25mA per Channel Typical at 100Mbps

  At 3.3V:
  - 2.6mA per Channel Typical at 1Mbps
  - 7.1mA per Channel Typical at 100Mbps

Safety Regulatory Approvals

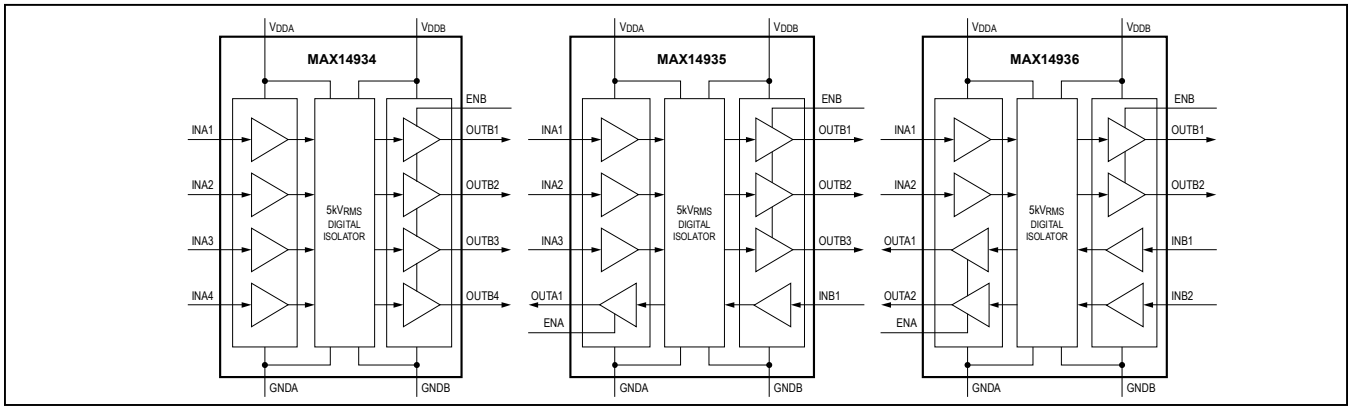
(see Safety Regulatory Approvals)

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-10

Applications

- Fieldbus Communications for Industrial Automation
- Isolated SPI, RS-232, RS-485/RS-422
- General Multichannel Isolation Applications
- Battery Management
- Medical Systems

Functional Diagram



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Absolute Maximum Ratings

V_{DDA} to GNDA, V_{DDB} to GNDB .....-0.3V to +6V
INA_, ENA to GNDA.....-0.3V to +6V
INB_, ENB to GNDB .....-0.3V to +6V
OUTA_ to GNDA .....-0.3V to (V_{DDA} + 0.3V)
OUTB_ to GNDB.....-0.3V to (V_{DDB} + 0.3V)
Short-Circuit Duration
(OUTA_ to GNDA, OUTB_ to GNDB) .....Continuous

Continuous Power Dissipation (T_A = +70°C)
Wide SOIC (derate 14.1mW/°C above +70°C) 1126.8mW
Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Wide SOIC
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....71°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....23°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Operating Supply Voltage	V_{DDA}	Relative to GNDA	1.71		5.5	V
	V_{DDB}	Relative to GNDB	1.71		5.5	V
Undervoltage Lockout Threshold	$V_{UVLO\_}$	$V_{DD\_}$ rising	1.45	1.58	1.71	V
Undervoltage Lockout Threshold Hysteresis	V_{UVLO_HYST}			50		mV

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (MAX14934_)	I_{DDA}	500kHz square wave	V_{DDA} = 5V		1.2	1.9	mA
			V_{DDA} = 3.3V		1.2	1.9	
			V_{DDA} = 2.5V		1.2	1.9	
			V_{DDA} = 1.8V		1.1	1.9	
		12.5MHz square wave (Note 3)	V_{DDA} = 5V		2.1	2.7	
			V_{DDA} = 3.3V		2	2.7	
			V_{DDA} = 2.5V		2	2.7	
			V_{DDA} = 1.8V		2	2.6	
		50MHz square wave (Note 3)	V_{DDA} = 5V		5	6.6	
			V_{DDA} = 3.3V		4.6	6.1	
			V_{DDA} = 2.5V		4.5	6.0	
			V_{DDA} = 1.8V		4.5	6.0	
	I_{DDB}	500kHz square wave	V_{DDB} = 5V		8.1	11.2	
			V_{DDB} = 3.3V		7.9	11.1	
			V_{DDB} = 2.5V		7.9	11.0	
			V_{DDB} = 1.8V		7.7	10.8	
		12.5MHz square wave (Note 3)	V_{DDB} = 5V		12.8	15.9	
			V_{DDB} = 3.3V		11.1	14.2	
			V_{DDB} = 2.5V		10.2	13.4	
			V_{DDB} = 1.8V		9.4	12.4	
		50MHz square wave (Note 3)	V_{DDB} = 5V		27.2	35.4	
			V_{DDB} = 3.3V		21.7	27.8	
			V_{DDB} = 2.5V		17.6	23.0	
			V_{DDB} = 1.8V		14.4	18.9	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (MAX14935_)	I_{DDA}	500kHz square wave	V_{DDA} = 5V		3.4	5.3	mA
			V_{DDA} = 3.3V		3.3	5.3	
			V_{DDA} = 2.5V		3.3	5.3	
			V_{DDA} = 1.8V		3.2	5.1	
		12.5MHz square wave (Note 3)	V_{DDA} = 5V		5.6	7.1	
			V_{DDA} = 3.3V		5	6.6	
			V_{DDA} = 2.5V		4.7	6.4	
			V_{DDA} = 1.8V		4.5	6.1	
		50MHz square wave (Note 3)	V_{DDA} = 5V		12.4	16.0	
			V_{DDA} = 3.3V		10.1	13.0	
			V_{DDA} = 2.5V		9.1	11.6	
			V_{DDA} = 1.8V		8.2	10.4	
	I_{DDB}	500kHz square wave	V_{DDB} = 5V		6.5	9.2	
			V_{DDB} = 3.3V		6.4	9.1	
			V_{DDB} = 2.5V		6.3	9.1	
			V_{DDB} = 1.8V		6.2	8.9	
		12.5MHz square wave (Note 3)	V_{DDB} = 5V		10.3	12.8	
			V_{DDB} = 3.3V		8.9	11.6	
			V_{DDB} = 2.5V		8.2	11.0	
			V_{DDB} = 1.8V		7.6	10.3	
		50MHz square wave (Note 3)	V_{DDB} = 5V		22.7	29.1	
			V_{DDB} = 3.3V		17.7	23.0	
			V_{DDB} = 2.5V		14.7	19.4	
			V_{DDB} = 1.8V		11.9	15.9	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (MAX14936_)	I_{DDA}	500kHz square wave	V_{DDA} = 5V		5.2	7.2	mA
			V_{DDA} = 3.3V		5.2	7.2	
			V_{DDA} = 2.5V		5.2	7.2	
			V_{DDA} = 1.8V		5	7.0	
		12.5MHz square wave (Note 3)	V_{DDA} = 5V		8.2	10.0	
			V_{DDA} = 3.3V		7.2	9.1	
			V_{DDA} = 2.5V		6.7	8.7	
			V_{DDA} = 1.8V		6.3	8.2	
		50MHz square wave (Note 3)	V_{DDA} = 5V		18	23.3	
			V_{DDA} = 3.3V		14.2	18.4	
			V_{DDA} = 2.5V		12.3	16.1	
			V_{DDA} = 1.8V		10.5	13.6	
	I_{DDB}	500kHz square wave	V_{DDB} = 5V		5.2	7.2	
			V_{DDB} = 3.3V		5.2	7.2	
			V_{DDB} = 2.5V		5.2	7.2	
			V_{DDB} = 1.8V		5	7.0	
		12.5MHz square wave (Note 3)	V_{DDB} = 5V		8.2	10.0	
			V_{DDB} = 3.3V		7.2	9.1	
			V_{DDB} = 2.5V		6.7	8.7	
			V_{DDB} = 1.8V		6.3	8.2	
		50MHz square wave (Note 3)	V_{DDB} = 5V		18	23.3	
			V_{DDB} = 3.3V		14.2	18.4	
			V_{DDB} = 2.5V		12.3	16.1	
			V_{DDB} = 1.8V		10.5	13.6	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS AND OUTPUTS							
Input High Voltage	V_{IH}	ENA, INA_ relative to GNDA		0.7 x V_{DDA}			V
		ENB, INB_ relative to GNDB		0.7 x V_{DDB}			
Input Low Voltage	V_{IL}	ENA, INA_ relative to GNDA	1.71V ≤ V_{DDA} ≤ 1.89V			0.6	V
			2.25V ≤ V_{DDA} ≤ 5.5V			0.8	
		ENB, INB_ relative to GNDB	1.71V ≤ V_{DDB} ≤ 1.89V			0.6	
			2.25V ≤ V_{DDB} ≤ 5.5V			0.8	
Input Hysteresis	V_{HYS}	$V_{INA\_}$ relative to GNDA or $V_{INB\_}$ relative to GNDB	MAX1493_A/D		410		mV
			MAX1493_B/E		410		
			MAX1493_C/F		80		
Input Leakage Current	I_L	$V_{INA\_}$ = 0 or V_{DDA}, $V_{INB\_}$ = 0 or V_{DDB}		-1		+1	µA
Input Capacitance	C_{IN}	INA_, INB_, f = 1MHz			2		pF
EN_ Pullup Current	I_{PU}			-4	-2.3	-1	µA
Output Voltage High	V_{OH}	$V_{OUTA\_}$ relative to GNDA, $I_{OUTA\_}$ = -4mA (Note 4)		V_{DDA} - 0.4			V
		$V_{OUTB\_}$ relative to GNDB, $I_{OUTB\_}$ = -4mA (Note 4)		V_{DDB} - 0.4			
Output Voltage Low	V_{OL}	$V_{OUTA\_}$ relative to GNDA, $I_{OUTA\_}$ = 4mA (Note 4)				0.4	V
		$V_{OUTB\_}$ relative to GNDB, $I_{OUTB\_}$ = 4mA (Note 4)				0.4	

Dynamic Electrical Characteristics (MAX1493_A/D)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CHANNELS							
Common-Mode Transient Immunity	CMTI	IN__ = GND_ or $V_{DD\_}$ (Note 5)			25		kV/µs
Maximum Data Rate	DR_{MAX}			1			Mbps
Minimum Pulse Width	PW_{MIN}	INA_ to OUTB_, INB_ to OUTA_				1	µs
Glitch Rejection		INA_ to OUTB_, INB_ to OUTA_			32		ns
Propagation Delay (Figure 1)	t_{PLH}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		38.2	54.1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		38.7	54.6	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		39.7	55.6	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		42.9	58.4	
	t_{PHL}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		38.6	55.3	
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		38.9	55.6	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		39.8	56.1	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		42.3	60.2	
Pulse-Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		0.4	4.5	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		0.2	4.3	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		0.1	3.9	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		0.6	4.7	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				26.6	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				26.6	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				26.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				26.9	
	t_{SPHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				27.9	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				27.7	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				27.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				29.7	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				6.7	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				6.7	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				6.7	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				6.7	
	t_{SCSHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				6.7	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				6.7	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				6.7	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				6.7	

Dynamic Electrical Characteristics (MAX1493_A/D) (Continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposing Direction)	t_{SCOLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				26.6	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				26.6	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				26.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				26.9	
	t_{SCOHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				27.9	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				27.7	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				27.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				29.7	
Rise Time (Figure 1)	t_R	OUTA_/ OUTB_, 10% to 90%, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Fall Time (Figure 1)	t_F	OUTA_/ OUTB_, 90% to 10%, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Enable to Data Valid	t_{EN}	ENA to OUTA_, ENB to OUTB_, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			5.1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			5.5	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			6.7	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			16.3	
Enable to Three-State	t_{TRI}	ENA to OUTA_, ENB to OUTB_, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			2.7	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			4.4	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			7.0	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			11.7	

Dynamic Electrical Characteristics (MAX1493_B/E)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CHANNELS							
Common-Mode Transient Immunity	CMTI	IN__ = GND_ or $V_{DD\_}$ (Note 5)			25		kV/µs
Maximum Data Rate	DR_{MAX}			25			Mbps
Minimum Pulse Width	PW_{MIN}	INA_ to OUTB_, INB_ to OUTA_				40	ns
Glitch Rejection		INA_ to OUTB_, INB_ to OUTA_			15		ns
Propagation Delay (Figure 1)	t_{PLH}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		20.9	27.5	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		21.4	28.7	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		22.4	31.2	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		25.7	36.9	
	t_{PHL}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		21.1	28.8	
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		21.5	29.8	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		22.3	31.9	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		24.9	37.4	
Pulse-Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		0.2	2.6	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		0.1	2.6	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		0.1	2.4	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		0.7	3.2	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				11.7	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				11.5	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				11.3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				13.6	
	t_{SPHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				9.8	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				9.8	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				11.1	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				14.4	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				3	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				3	
	t_{SCSHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				3	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				3	

Dynamic Electrical Characteristics (MAX1493_B/E) (Continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel to Channel (Opposing Direction)	t_{SCOLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				11.7	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				11.5	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				11.3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				13.6	
	t_{SCOHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				9.8	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				9.8	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				11.1	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				14.4	
Rise Time (Figure 1)	t_R	OUTA_/ OUTB_, 10% to 90%, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Fall Time (Figure 1)	t_F	OUTA_/ OUTB_, 90% to 10%, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Enable to Data Valid	t_{EN}	ENA to OUTA_, ENB to OUTB_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			5.1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			5.5	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			6.7	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			16.3	
Enable to Three-State	t_{TRI}	ENA to OUTA_, ENB to OUTB_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			2.7	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			4.4	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			7.0	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			11.7	

Dynamic Electrical Characteristics (MAX1493_C/F)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CHANNELS							
Common-Mode Transient Immunity	CMTI	IN__ = GND_ or $V_{DD\_}$ (Note 5)			25		kV/µs
Maximum Data Rate	DR_{MAX}			150			Mbps
Minimum Pulse Width	PW_{MIN}	INA_ to OUTB_, INB_ to OUTB_				6.67	ns
Propagation Delay (Figure 1)	t_{PLH}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		5.1	7.5	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		5.2	8.1	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		5.8	9.7	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		8.1	14	
	t_{PHL}	INA_ to OUTB_, INB_ to OUTA_, C_L = 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		4.9	7.4	
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		5.3	8.3	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		5.9	10.2	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		8.2	14.9	
Pulse-Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		0.2	1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		0.1	1	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		0.1	1	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		0.1	1	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				3.0	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3.3	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				4.3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				7.1	
	t_{SPHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				2.8	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3.4	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				4.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				7.9	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				0.9	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				1.2	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				1.4	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				1.6	
	t_{SCSHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				0.9	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				1.2	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				1.4	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				1.6	

Dynamic Electrical Characteristics (MAX1493_C/F) (continued)

(V_{DDA} - V_{GNDA} = +1.71V to +5.5V, V_{DDB} - V_{GNDB} = +1.71V to +5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposing Direction)	t_{SCOLH}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				3	ns
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3.3	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				4.3	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				7.1	
	t_{SCOHL}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V				2.8	
		3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V				3.4	
		2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V				4.6	
		1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V				7.9	
Rise Time (Figure 1)	t_R	OUTA_/ OUTB_, 10% to 90%, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Fall Time (Figure 1)	t_F	OUTA_/ OUTB_, 90% to 10%, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V		2		ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V		2		
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V		2		
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V		2		
Enable to Data Valid	t_{EN}	ENA to OUTA_, ENB to OUTB_, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			5.1	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			5.5	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			6.7	
			1.71V ≤ V_{DDA}, V_{DDB} ≤ 1.89V			16.3	
Enable to Three-State	t_{TRI}	ENA to OUTA_, ENB to OUTB_, C_L= 15pF	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			2.7	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			4.4	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			7.0	
			V_{DDA}, V_{DDB} ≤ 1.89V			11.7	
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	V_{DDA}, V_{DDB} = 5.0V			140		ps
		V_{DDA}, V_{DDB} = 3.3V			130		
		V_{DDA}, V_{DDB} = 2.5V			140		
		V_{DDA}, V_{DDB} = 1.8V			160		

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, All Pins		±4		kV

Note 2: All devices are 100% production tested at T_A = +125°C. Specifications over temperature are guaranteed by design.
Note 3: Not production tested. Guaranteed by design.
Note 4: All currents into the device are positive. All currents out of the device are negative.
Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

Safety Regulatory Approvals

UL
The MAX14934–MAX14936 are certified under UL1577. For more details, refer to File E351759.
Rated up to 5000V$_{RMS}$ isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX14934/MAX14936 are certified up to 5000V$_{RMS}$ for single protection. For more details, refer to File 351759.
VDE
The MAX14934–MAX14936 is certified to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12. For details, see file ref. 5015017-4880-0001/217630/EC22/SCT. Basic Insulation, Maximum Transient Isolation Voltage 8400V$_{PK}$, Maximum Working Voltage 848V$_{RMS}$

IEC Insulation Testing

TUV
The MAX14934/MAX14936 are tested under TUV.
IEC60950-1: Up to 1200VP (848V$_{RMS}$) working voltage for basic insulation.
IEC61010-1 (ed. 3): Up to 848V$_{RMS}$ working voltage for basic insulation. For details, see Technical Report number 095-72100581-100.
IEC60601-1 (ed. 3): For details see Technical Report number 095-72100581-200.
Basic insulation 1 MOOP, 1200V$_{PK}$ (848V$_{RMS}$)
Withstand isolation voltage for 60s (Viso) 5000V$_{RMS}$

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	2250	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}		1200	V_P
Maximum Working Isolation Voltage	V_{IOWM}		848	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	8400	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s	5000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation 1.2/50µs pulse	10	kV
Insulation Resistance	R_S	T_A = +150°C V_{IO} = 500V	> 10^{12}	Ω
Barrier Capacitance Input to Output (Note 6)	CIO	f_{SW} = 1MHz	2	pF
Minimum Creepage Distance	CPG	Wide SOIC	8	mm
Minimum Clearance Distance	CLR	Wide SOIC	8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Resistance Index	CTI	Material Group II (IEC 60112)	575	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6. Capacitance is measured with all pins on side A and side B tied together.

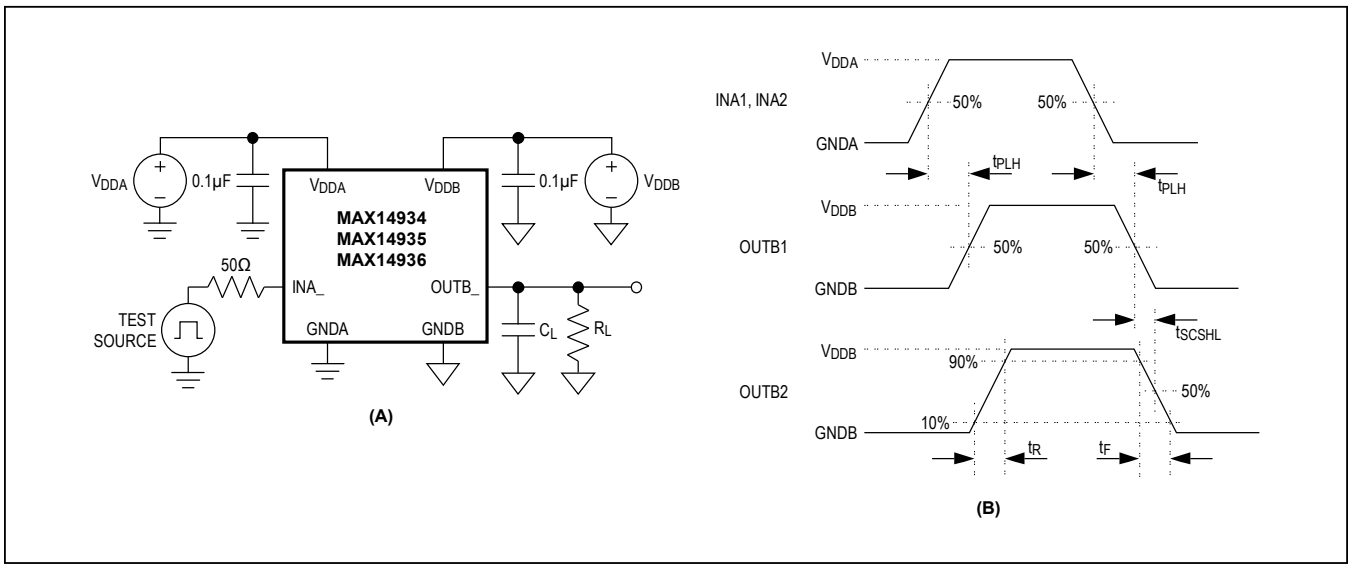
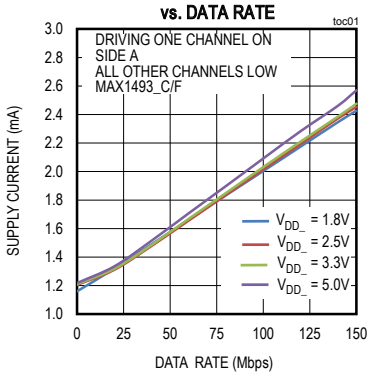


Figure 1. Test Circuit (A) and Timing Diagram (B)

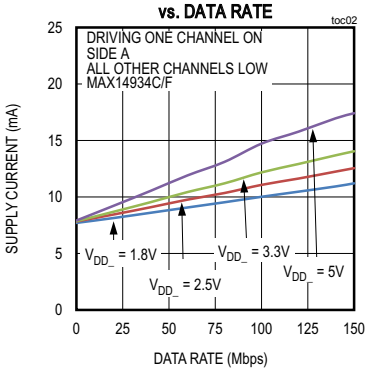
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

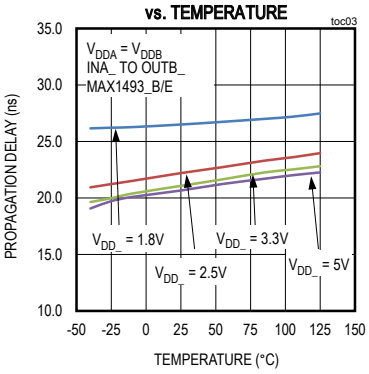
SIDE A SUPPLY CURRENT vs. DATA RATE



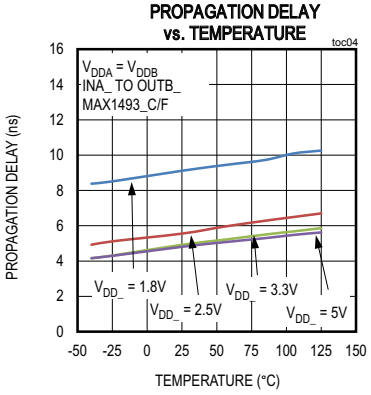
SIDE B SUPPLY CURRENT vs. DATA RATE



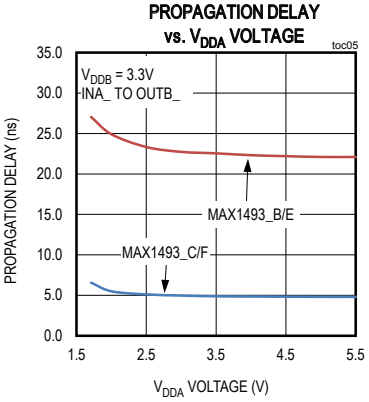
PROPAGATION DELAY vs. TEMPERATURE



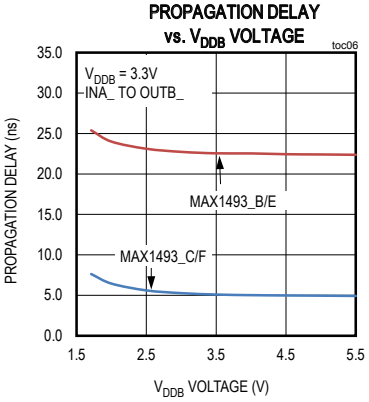
PROPAGATION DELAY vs. TEMPERATURE



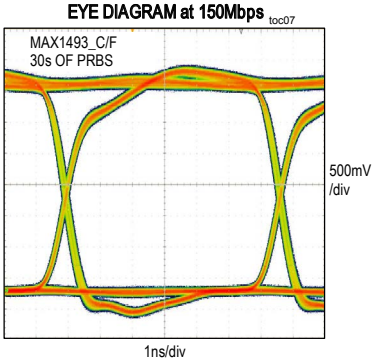
PROPAGATION DELAY vs. V_{DDA} VOLTAGE



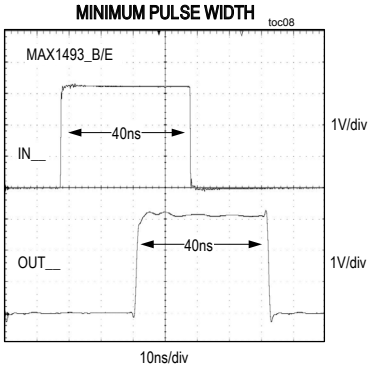
PROPAGATION DELAY vs. V_{DDB} VOLTAGE



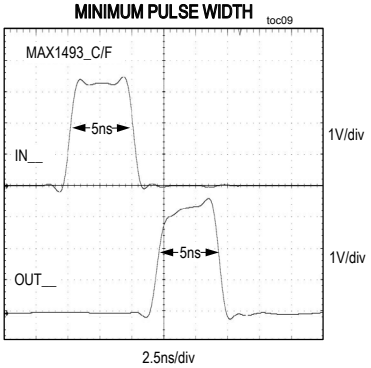
EYE DIAGRAM at 150Mbps



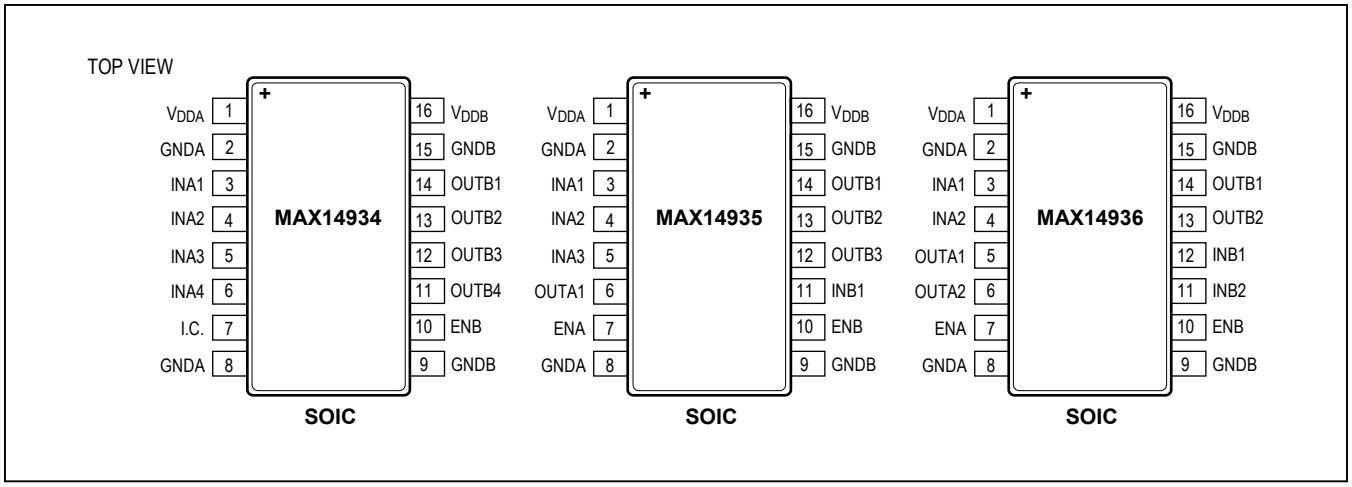
MINIMUM PULSE WIDTH



MINIMUM PULSE WIDTH



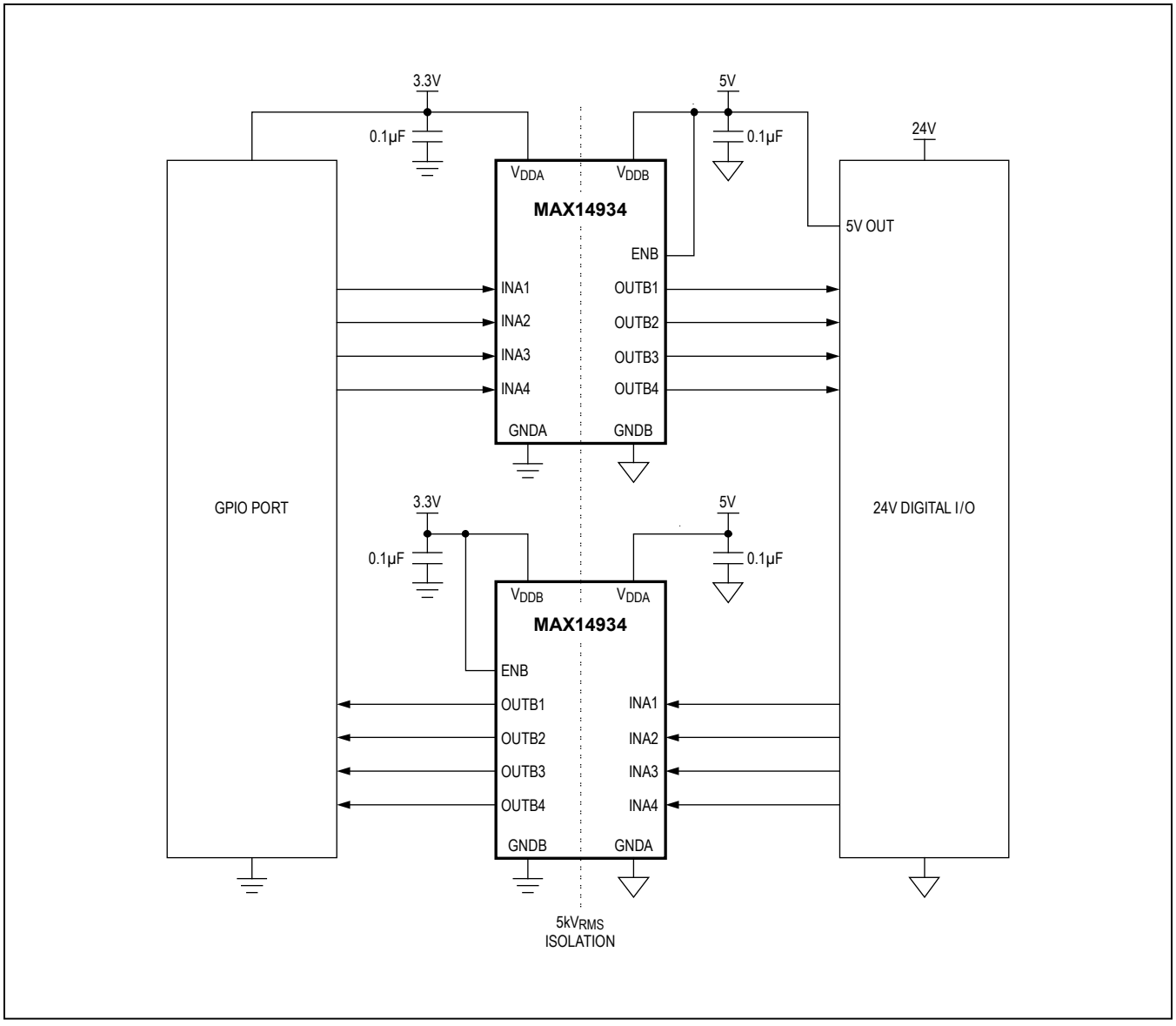
Pin Configurations



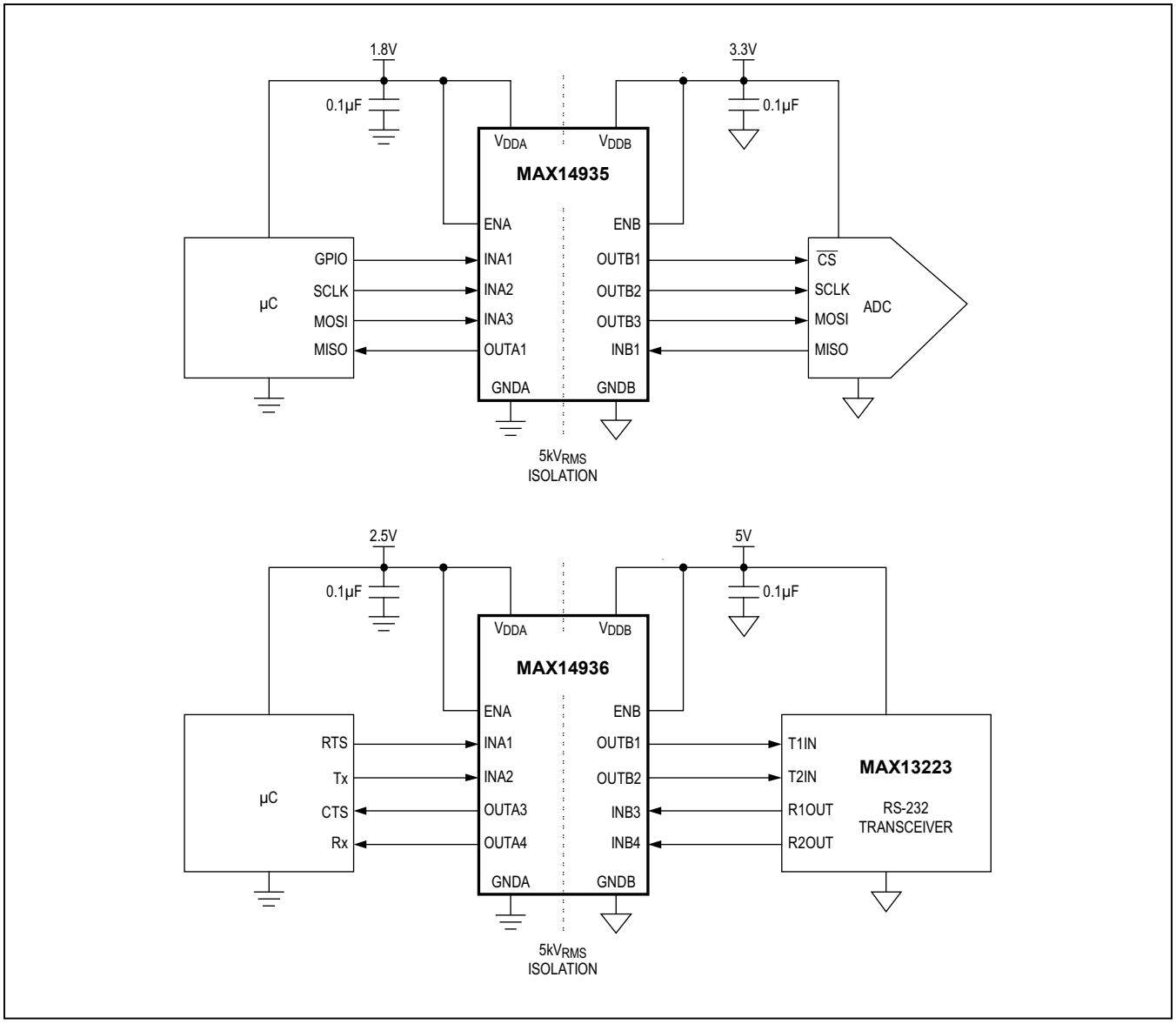
Pin Description

PIN			NAME	FUNCTION	VOLTAGE RELATIVE TO
MAX14934	MAX14935	MAX14936			
1	1	1	V_{DDA}	Power Supply. Bypass V_{DDA} with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDA
2, 8	2, 8	2, 8	GNDA	Ground Reference for Side A	—
3	3	3	INA1	Logic Input 1 on Side A. INA1 corresponds to OUTB1.	GNDA
4	4	4	INA2	Logic Input 2 on Side A. INA2 corresponds to OUTB2.	GNDA
5	5	—	INA3	Logic Input 3 on Side A. INA3 corresponds to OUTB3.	GNDA
6	—	—	INA4	Logic Input 4 on Side A. INA4 corresponds to OUTB4.	GNDA
7	—	—	I.C.	Internally Connected. Leave unconnected or connect to GNDA or V_{DDA}.	—
—	6	5	OUTA1	Logic Output 1 on Side A	GNDA
—	—	6	OUTA2	Logic Output 2 on Side A	GNDA
—	7	7	ENA	Active-High Enable for Side A. ENA has an internal 2µA pullup to V_{DDA}.	GNDA
9, 15	9, 15	9, 15	GNDB	Ground Reference for Side B	—
10	10	10	ENB	Active-High Enable for Side B. ENB has an internal 2µA pullup to V_{DDB}.	GNDB
11	—	—	OUTB4	Logic Output 4 on Side B	GNDB
—	11	12	INB1	Logic Input 1 on Side B. INB1 corresponds to OUTA1.	GNDB
—	—	11	INB2	Logic Input 2 on Side B. INB2 corresponds to OUTA2.	GNDB
12	12	—	OUTB3	Logic Output 3 on Side B	GNDB
13	13	13	OUTB2	Logic Output 2 on Side B	GNDB
14	14	14	OUTB1	Logic Output 1 on Side B	GNDB
16	16	16	V_{DDB}	Power Supply. Bypass V_{DDB} with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDB

Typical Operating Circuit



Typical Operating Circuit (continued)



Detailed Description

The MAX14934–MAX14936 are a family of four-channel digital isolators. The MAX14934–MAX14936 family transfers digital signals between circuits with different power domains. The devices are rated for 5kV$_{RMS}$ isolation voltage for 60 seconds. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

The MAX14934–MAX14936 family offers three unidirectional channel configurations for design convenience. The MAX14934 features four channels transferring digital signals in one direction for applications such as isolated digital I/O. The MAX14935 has three channels transmitting data in one direction and one channel transmitting in the opposite direction, making it ideal for applications such as isolated SPI and RS-485 communication. The MAX14936 provides further design flexibility with two channels in each direction for isolated RS-232 or other applications.

Devices are available with data rates from DC up to 1Mbps (A/D versions), 25Mbps (B/E versions), or 150Mbps (C/F versions). Each device can also be ordered with default-high or default-low outputs. This is the state an output will go to when the input side of the device is unpowered.

The devices have two supply inputs, V_{DDA} and V_{DDB}, that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The MAX14934–MAX14936 family also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The MAX14934–MAX14936 family provides galvanic isolation for digital signals that are transmitted between two ground domains. Up to 1200V$_{PEAK}$ of continuous isolation is supported, as well as transient differences of up to 5kV$_{RMS}$ for up to 60 seconds.

Level Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX14934–MAX14936 family to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the MAX14934–MAX14936 is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each device features four unidirectional channels that operate independently with guaranteed data rates from DC up to 1Mbps (A/D versions), 25Mbps (B/E versions), or 150Mbps (C/F versions). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the status of the inputs (Table 1). Figure 2 through Figure 5 show the behavior of the outputs during power-up and power-down.

Applications Information

Power-Supply Sequencing

The MAX14934–MAX14936 do not require special power-supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

Table 1. Output Behavior During Undervoltage Conditions

V_{IN}	V_{DDA}	V_{DDB}	ENA	ENB	V_{OUTA}	V_{OUTB}
1	Powered	Powered	1	1	1	1
			0	0	Hi-Z	Hi-Z
0	Powered	Powered	1	1	0	0
			0	0	Hi-Z	Hi-Z
X	Undervoltage	Powered	1	1	Default	Default
			0	0	Hi-Z	Hi-Z
X	Powered	Undervoltage	1	1	Default	Default
			0	0	Hi-Z	Hi-Z

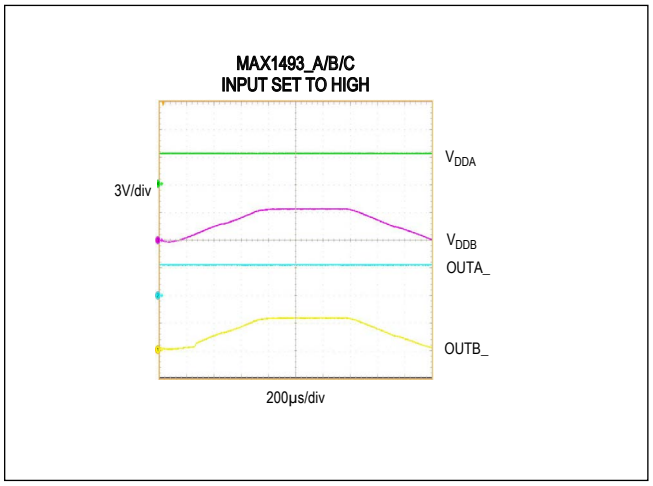


Figure 2. Undervoltage Lockout Behavior (MAX1493_A/BC High)

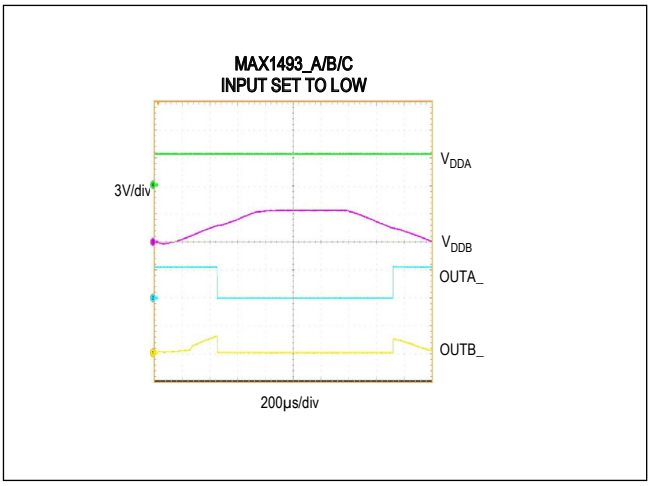


Figure 3. Undervoltage Lockout Behavior (MAX1493_A/BC Low)

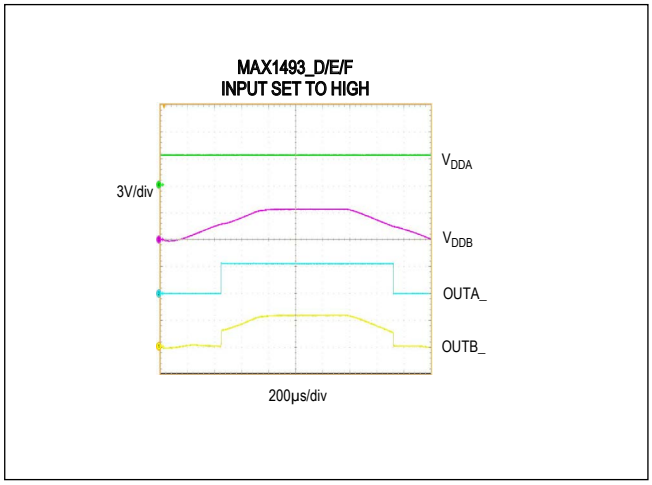


Figure 4. Undervoltage Lockout Behavior (MAX1493_D/E/F High)

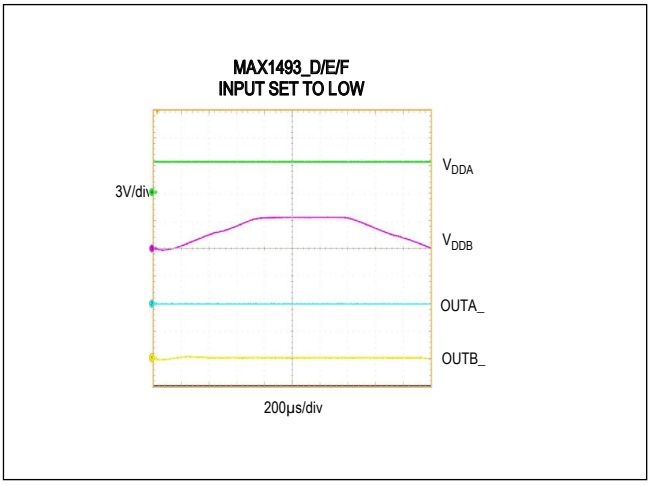


Figure 5. Undervoltage Lockout Behavior (MAX1493_D/E/F Low)

Ordering Information/Selector Guide

PART	CHANNEL CONFIGURATION	DATA RATE (Mbps)	OUTPUT	TEMP RANGE (°C)	PIN-PACKAGE
MAX14934AAWE+	4/0	1	Default high	-40 to +125	16 wide SOIC
MAX14934BAWE+	4/0	25	Default high	-40 to +125	16 wide SOIC
MAX14934CAWE+	4/0	150	Default high	-40 to +125	16 wide SOIC
MAX14934DAWE+	4/0	1	Default low	-40 to +125	16 wide SOIC
MAX14934EAWE+	4/0	25	Default low	-40 to +125	16 wide SOIC
MAX14934FAWE+	4/0	150	Default low	-40 to +125	16 wide SOIC
MAX14935AAWE+	3/1	1	Default high	-40 to +125	16 wide SOIC
MAX14935BAWE+	3/1	25	Default high	-40 to +125	16 wide SOIC
MAX14935CAWE+	3/1	150	Default high	-40 to +125	16 wide SOIC
MAX14935DAWE+	3/1	1	Default low	-40 to +125	16 wide SOIC
MAX14935EAWE+	3/1	25	Default low	-40 to +125	16 wide SOIC
MAX14935FAWE+	3/1	150	Default low	-40 to +125	16 wide SOIC
MAX14936AAWE+	2/2	1	Default high	-40 to +125	16 wide SOIC
MAX14936BAWE+	2/2	25	Default high	-40 to +125	16 wide SOIC
MAX14936CAWE+	2/2	150	Default high	-40 to +125	16 wide SOIC
MAX14936DAWE+	2/2	1	Default low	-40 to +125	16 wide SOIC
MAX14936EAWE+	2/2	25	Default low	-40 to +125	16 wide SOIC
MAX14936FAWE+	2/2	150	Default low	-40 to +125	16 wide SOIC

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 Wide SOIC	W16M+8	**21-0042**	**90-0107**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—
1	12/14	Removed future product notation from MAX14935DAWE+ in *Ordering Information* table, changed “basic insulation” to “single protection” in *Safety Regulatory Approvals* table, and updated third bullet of *Many Options Support Broad Applications* in *Features and Benefits* section.	1, 13, 22
2	3/15	Changed future product status for: MAX14934DAWE+, MAX14936AAWE+, MAX14936BAWE+, MAX14936DAWE+, MAX14936EAWE+, and MAX14936FAWE+.	22
3	7/15	Updated *Benefits and Features* section, *Safety Regulatory Approvals*, *Insulation Characteristics* tables, and *Pin Configuration* tables.	1, 13, 14, 16
4	4/16	Fixed typos, updated *Safety Regulatory Approvals*, and updated *Ordering Information/ Selection Guide*.	1, 13, 14, 21
5	5/16	Updated TUV information and created *IEC Insulation Testing* table	1, 13
6	1/17	Updated Figure 1 text and removed VDE pending	1, 13, 14

